Amendments to the Claims

Please amend claims 1 - 10 as follows:

1. (Currently Amended) ~~An integrated circuit device comprising elements, wherein the elements comprise characteristics and parameters in accordance with a circuit model, wherein the circuit model comprises:~~

A memory for access by a circuit simulation program comprising:

a circuit model of a black box circuit stored in the memory, the circuit model comprising

at least one output node;

a first and second current function;

a first voltage function;

a first, second, and third capacitance function; and

an internal impedance function;

wherein the output node has a value that is a function of the first and second current function, the first voltage function, the first, second and third capacitance functions and the internal impedance function ~~collectively~~.

2. (Currently Amended) The circuit model ~~device~~ of claim 1 wherein the first and second current functions are subsequently functions of the input node voltage value and the output node voltage value.

3. (Currently Amended) The circuit model ~~device~~ of claim 2 wherein the first, second, and third capacitance functions and the impedance function are each functions of the input and output voltage values.

4. (Currently Amended) The circuit model ~~device~~ of claim 1, further comprising:

an output load function, wherein the output load function is a function of a near capacitor

function, a resistor function, and a far capacitor function~~, collectively~~.

5. (Currently Amended) The circuit model ~~device~~ of claim 1, wherein the first current function is a function of a p-block behavioral model, and the second current function is a function of an n-block behavioral model.

6. (Currently Amended) The circuit model ~~device~~ of claim 5 wherein the first current function is a function of each of the input and output node values of the black box circuit~~, collectively~~.

7. (Currently Amended) The circuit model ~~device~~ of claim 5 wherein a plurality of the first current functions are arranged in parallel and each ~~first current function~~ is configured to be functionally dependent on a ~~first~~ portion of a plurality of input node voltage values and a ~~second~~ portion of a plurality of output node voltage values;

and a plurality of the second current functions are arranged in parallel and each ~~second current function~~ is configured to be functionally dependent on a ~~third~~ portion of the plurality of input node voltage values and a ~~fourth~~ portion of the plurality of output node voltage values.

8. (Currently Amended) ~~An integrated circuit device comprising elements, wherein the elements comprise characteristics and parameters in accordance with a circuit model, wherein the circuit model comprises:~~

A memory for access by a circuit simulation program comprising:

a circuit model of a black box circuit stored in the memory, the circuit model comprising,

an ideal current source connecting an output node to a voltage supply;

a first capacitor connected to the input node and the output node;

an input capacitor connected to the input node and to ground;

an output capacitor connected to the output node and ground; and

an internal impedance, connected to the output node and ground~~.~~;

wherein the ideal current source, the capacitance of each capacitor and the internal impedance are each functions of the input node and output node voltage.

9. (Canceled)

10. (Currently Amended) The circuit model ~~device~~ of ~~claim 9~~ claim 8, further comprising an output load, having a near capacitor, a resistor, and a far capacitor.

11. (Withdrawn) A method of modeling an IC that provides output waveforms, comprising the steps of:

translating a model of the IC comprising ideal current sources and capacitors into a differential equation which is implicit with respect to output voltages;

supplying values of the model's elements at a sufficient I/O voltages to cover the desired range of I/O node voltages;

resimulating the model by solving the differential equation through an ODE solver, given an input waveform, the element values and an output load.

12. (Withdrawn) The method of modeling an IC of claim 11 also comprising the step of:

storing generalization equations and solving the generalization equations to obtain model element values.

13. (Withdrawn) The method of modeling an IC of claim 11 also comprising the step of:

performing measurements in order to obtain the model element values.

14. (Withdrawn) The method of claim 11 also comprising the steps of:

interpolating of element values in the space of I/O node voltages;

manipulating element values such as time or voltage-threshold-based delay, averaging or clipping.

15. (Withdrawn) The method of claim 12 also comprising the step of:

solving the generalization equations using interpolated parameters and externally specified environmental parameters to obtain model element values.

16. (Withdrawn) The method of claim 11 also comprising the step of:

at each time step during solution of the ODE, determining the output load by having the ODE solver call a callback function requesting the load current by providing to the callback function the time and output node voltage.

17. (Withdrawn) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for modeling an IC, the method steps comprising:

translating a model of the IC comprising ideal current sources and capacitors into a differential equation which is implicit with respect to output voltages;

supplying values of the model's elements at a sufficient I/O voltages to cover the desired range of I/O node voltages;

re-simulating the model by solving the differential equation through an ODE solver, given an input waveform, the element values and an output load.

18. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

storing generalization equations and solving the generalization equations to obtain model element values.

19. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

performing measurements in order to obtain the model element values.

20. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

interpolating of element values in the space of I/O node voltages;

manipulating element values for environmental parameters such as time or voltage-threshold-based delay, averaging, or clipping.

21. (Withdrawn) The program storage device of claim 18 wherein the method steps also comprise:

solving the generalization equations using interpolated parameters and externally specified environmental parameters to obtain model element values.

22. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

at each time step of the input waveform, determining the output load by having the ODE solver call a callback function requesting the load current by providing to the callback function the time and output node voltage.

23. (New) A method of simulating a black box circuit while hiding circuit details, comprising the steps of:

translating a circuit model of the black box circuit, having at least one current source and at least one capacitor, into an implicit ordinary differential equation (ODE);

supplying a plurality of final element values to the ODE, each of the final element values corresponding to a value associated with the current source response or a value associated with the capacitor response when an I/O node voltage is applied to the circuit model; and

solving the ODE using an ODE solver, given a predetermined input waveform, the plurality of final element values, and an output load current.

24. (New) The method of claim 23 further comprising the step of:

generating a plurality of generalization equations using a plurality of predetermined element value equation parameters; and

resolving the generalization equations to obtain a plurality of base element values which correspond to the response of the circuit model under predetermined conditions.

25. (New) The method of claim 24 further comprising the step of:

solving the generalization equations using externally applied environmental parameters to obtain a plurality of base element values; and

filtering the base element values to obtain a plurality of final element values.

26. (New) The method of claim 23 further comprising the step of:

measuring the actual element values during simulation of the circuit model to obtain the plurality of final element values used by the ODE solver.

27. (New) The method of claim 23 further comprising the steps of:

interpolating between a predetermined plurality of stored element values which correspond to the response of the circuit model at predetermined I/O node voltages to determine a plurality of base element values at desired I/O node voltages which are not stored.

28. (New) The method of claim 27 further comprising the step of:

filtering the base element values to obtain a plurality of final element values.

29. (New) The method of claim 23 further comprising the step of:

determining the output load current at each of a plurality of time intervals;

wherein for each time interval, the ODE solver provides a specific time value, dependant upon the time interval, and an output node voltage value to a load callback function; and the load callback function returning the output load current.

30. (New) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for simulating a black box circuit such that the circuit details are hidden, the method steps comprising:

translating a circuit model of the black box circuit, having at least one current source and at least one capacitor, into an implicit ordinary differential equation (ODE);

supplying a plurality of final element values to the ODE, each of the final element values corresponding to a value associated with the current source response or a value associated with the capacitor response when an I/O node voltage is applied to the circuit model; and

solving the ODE using an ODE solver, given a predetermined input waveform, the plurality of final element values, and an output load current.

31. (New) The program storage device of claim 30 wherein the method steps also comprise:

generating a plurality of generalization equations using a plurality of predetermined element value equation parameters.

32. (New) The program storage device of claim 31, wherein the method steps also comprise:

solving the generalization equations using externally applied environmental parameters to obtain a plurality of base element values; and

filtering the base element values to obtain a plurality of final element values.

33. (New) The program storage device of claim 30 wherein the method steps also comprise:

measuring the actual element values during simulation of the circuit model to obtain the plurality of final element values used by the ODE solver.

34. (New) The program storage device of claim 30 wherein the method steps also comprise:

interpolating between a predetermined plurality of stored element values which correspond to the response of the circuit model at predetermined I/O node voltages to determine a plurality of base element values at desired I/O node voltages which are not stored.

35. (New) The program storage device of claim 34, wherein the method steps also comprise:

filtering the base element values to obtain a plurality of final element values.

36. (New) The program storage device of claim 30 wherein the method steps also comprise:

determining the output load current at each of a plurality of time intervals;
wherein for each time interval, the ODE solver provides a specific time value, dependant upon the time interval, and an output node voltage value to a load callback function; and the load callback function returning the output load current.